

Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice. Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.

15CS72

c. Consider the following reservation table for a 4-stage pipeline with a clock cycle $\tau = 2ns$.



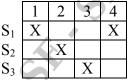
- i) What are the forbidden latencies and the initial collision vector?
- ii) Draw the state transition diagrams for scheduling the pipeline.
- iii) Determine the MAL associated with shorted greedy cycle.
- iv) Determine the pipeline throughput corresponding to the MAL and given τ .
- v) Determine the lower bound on the MAL for this pipeline, have you obtained the optimal latency from the above state diagram.

(06 Marks)

(05 Marks)

OR

- a. With state diagrams, explain the state transition diagram for a pipeline unit. (05 Marks)
- b. Explain the Tomasulo's algorithm for dynamic instruction scheduling.
- c. Consider the following pipeline reservation table:



i) What are the forbidden latencies?

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- ii) Draw the state transition diagram.
- iii) List all the simple cycles and greedy cycles.
- iv) Determine the optimal constant latency cycle and the minimal average latency.
- v) Let the pipeline clock period be $\tau = 20$ ns. Determine the throughput of this pipeline.

(06 Marks)

Module-4

7 a. With a neat diagram, explain the bus systems at board level, back plane and I/O level.

(08 Marks)

b. Define cache coherence problem. Describe cache coherence problems in data sharing and process migration. (08 Marks)

OR

- 8 a. Explain Goodman's write once cache coherence protocol using write invalidate policy on write back caches. (08 Marks)
 - b. With a neat diagram, explain C-access and S-access organization for an m-way interleaved memory. (08 Marks)

Module-5

9 a. With a neat sketch, explain the compilation phases in parallel code-generation. (08 Marks)
b. Discuss in brief difference between local and global branch prediction and how a 2 bit branch selector may be used per branch to select between two. Explain with transition diagram. (08 Marks)

OR

- 10 a. Explain the different loop transformations and discuss how to apply to them for loop vectorization or parallelism. (08 Marks)
 - b. Describe in brief the structure of the reorder buffer and how the use of reorder buffer addresses the various types of dependences in the program. (08 Marks)

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